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#4

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Chaitanya S. Rajguru

Art Unit : Unknown

Serial No. : 09/993,336

Examiner : Unknown

Filed : November 13, 2001

Title : FLASH MEMORY PROGRAM AND ERASE OPERATIONS

Attention: Official Draftsman

Commissioner for Patents

Washington, D.C. 20231

TRANSMITTAL OF FORMAL DRAWINGS

Please substitute the enclosed four (4) sheets of formal drawings for the corresponding drawings presently in the application.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/29/02

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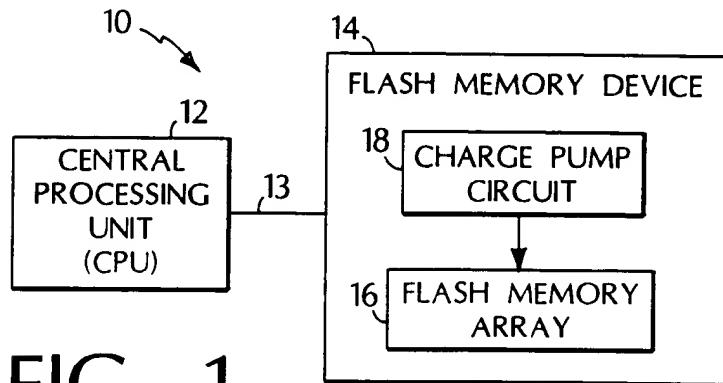


FIG. 1

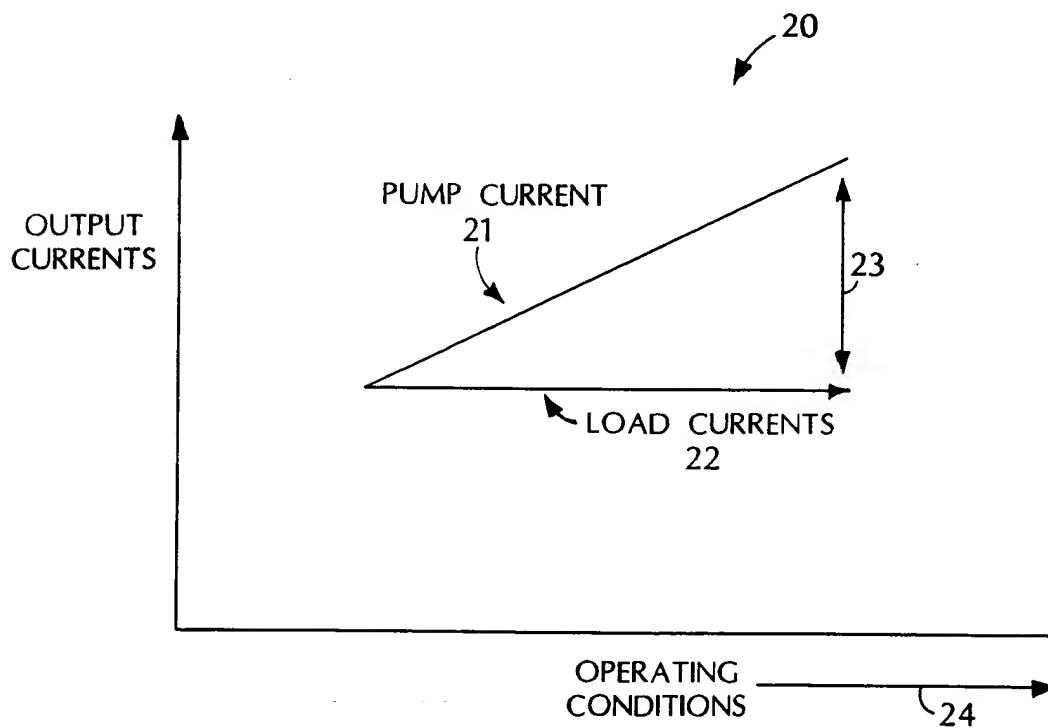


FIG. 2

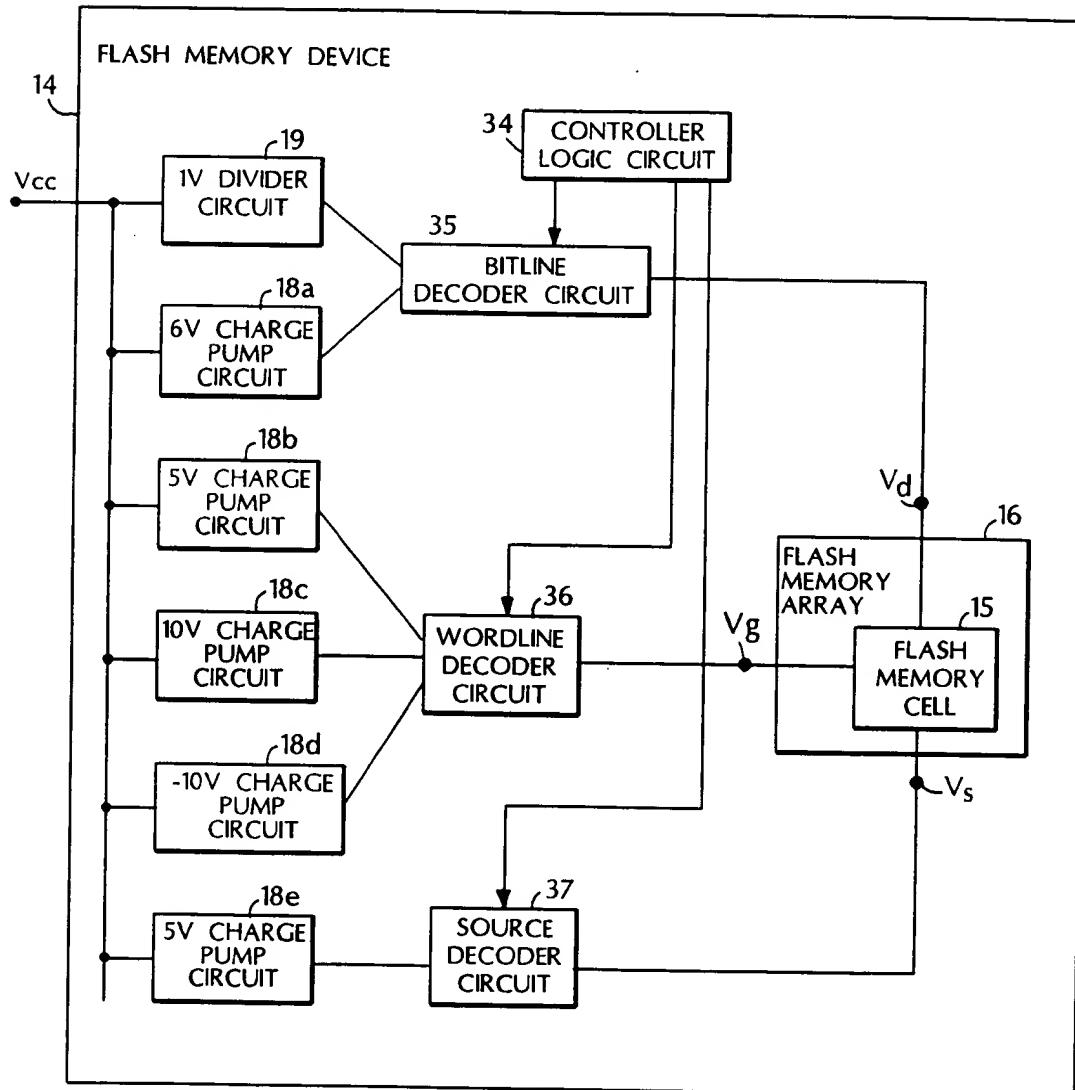


FIG. 3A

TABLE: VOLTAGE FOR PROCESSING FLASH DEVICE

	<u>V_g</u>	<u>V_d</u>	<u>V_s</u>
<u>PROGRAM</u>	10	6	0
<u>ERASE</u>	-10	0	FLOAT
<u>READ</u>	5	1	0

FIG. 3B

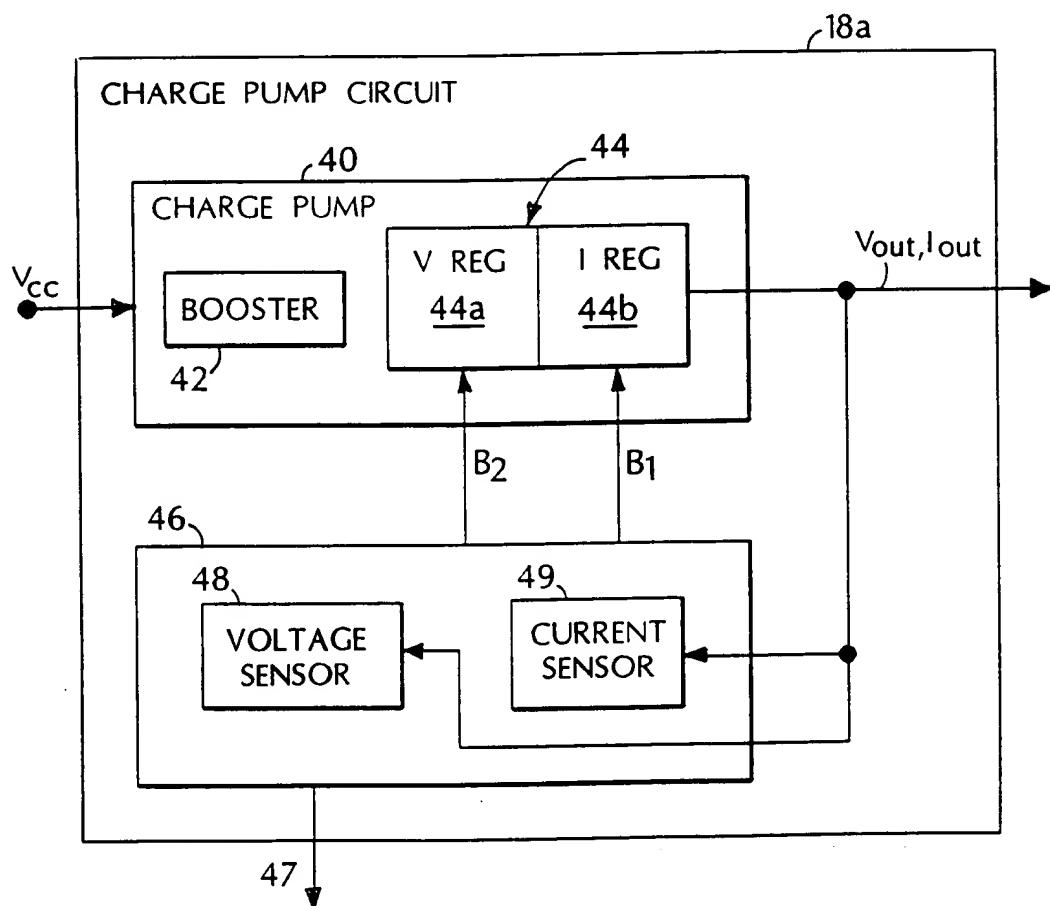


FIG. 4

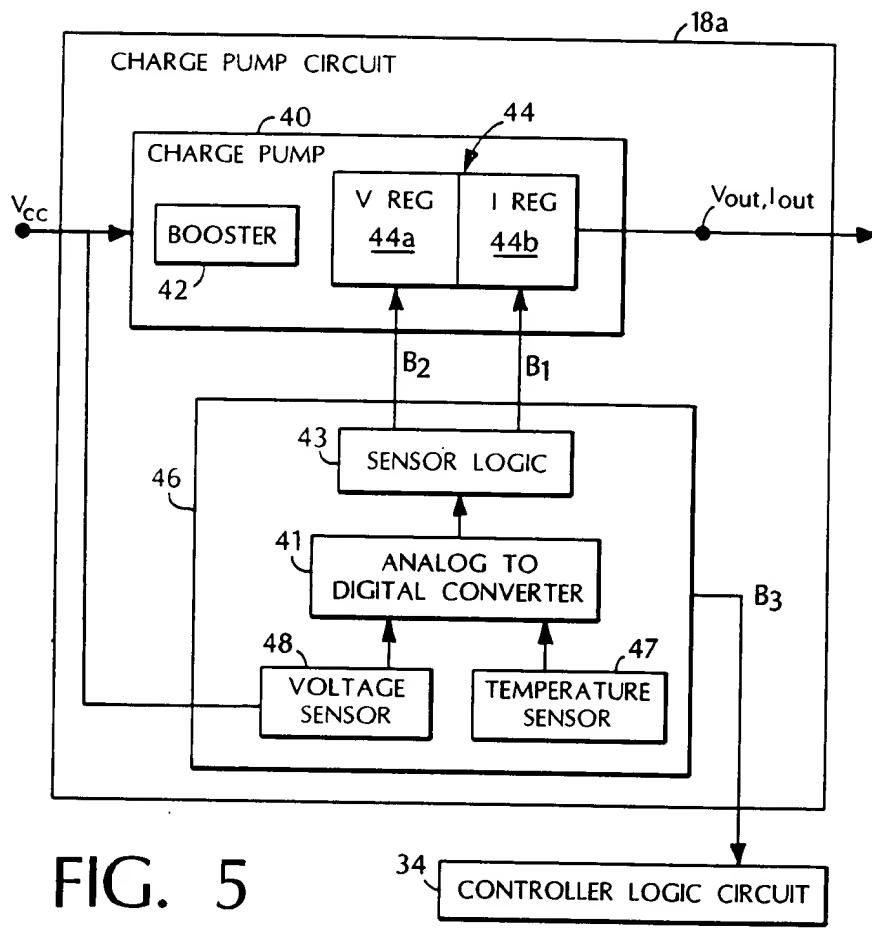


FIG. 5

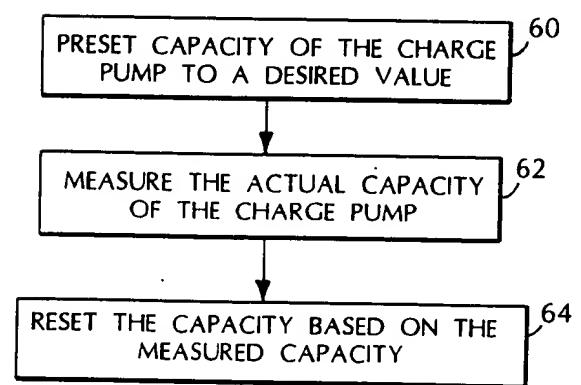


FIG. 6